A High Power and High Efficiency Amplifier With Controlled Second-harmonic Source Impedance

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SUMMARY

A novel technology that drastically improves output power and efficiency of amplifiers has been developed. A record high 74% power added efficiency (PAE) with an output power (Pout) of 31.4dBm (1.4W) has been achieved from an ion-implanted GaAs MESFET at a low supply voltage of 3.5V and 930MHz, by optimally terminating second-harmonic source impedance as well as second-harmonic load impedance. By using this technology, a small sized (0.4cc) power amplifier module for cellular phones has been developed. It has realized a high PAE of 66% with Pout of 31dBm (1.25W) under the condition of 3.5V around 915-945 MHz band.

INTRODUCTION

Advanced high performance hand-held phones require high efficiency power amplifiers with a low supply voltage. In order to obtain high efficiency, many different types of power amplifiers such as Class F [1] and tuned class-B have been reported. In tuned class-B amplifier, second-harmonic load impedance is terminated with a short circuit. The theoretical drain efficiency is reported to be 86% [2].

In another approach, a high efficiency amplifier by inputting a quasi-square voltage wave into a FET gate has also reported [3]. However this technology has difficulty in applying to small sized power amplifiers because the quasi-square voltage wave has to be synthesized outside the amplifier. We have found that a voltage wave inputted into a FET gate is well controlled from a sinusoidal wave to a quasi-square wave by optimally terminating second-harmonic source impedance with a short circuit. In this paper, we describe the effects of tuning second harmonic source impedance on output power and efficiency of amplifiers at 900MHz band. The gate voltage and current waveforms analyzed by harmonic balance simulation are discussed.

POWER MESFET

A GaAs MESFET with a total gate width (Wg) of 12mm was fabricated by an ion-implanted channel recessed-gate technology. By optimizing the device dimension and the fabrication processes, low knee voltage (Vk) of I-V characteristics and high gate-to-drain breakdown voltage (BVgd) have been attained [4]. The gate-source spacing (Lgs), the gate length (Lg) and the gate-drain spacing (Lgd) are 0.5-0.6-1.0 μm (= Lgs - Lg - Lgd). An active channel is formed by implantation of Si ions at 80KeV at a dose of 3.9×10^{12} cm^{-2}. The FET has Vk of 1.2V, and has BVgd of more than 20V at a gate current density of 1mA/mm. The saturation drain current at Vg = 0V (Idss) and pinch-off voltage are 3.0A and -2.8V, respectively.

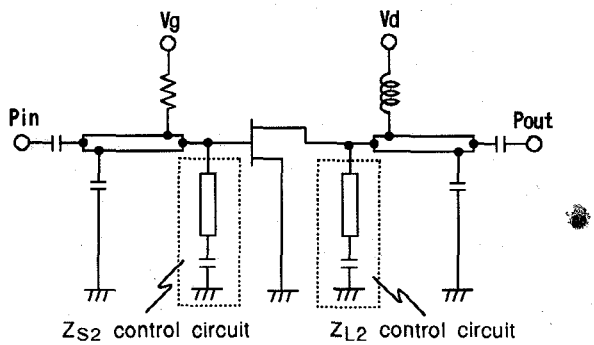

Fig. 1. A Circuit diagram of the newly developed power amplifier. Source and load second-harmonic impedances (Z_{S2}, Z_{L2}) were optimally controlled with approximate short circuits.

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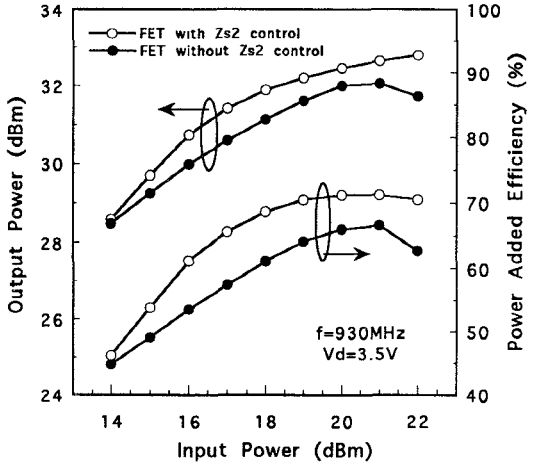


Fig. 2. Measured Pout and PAE of the FET as a function of Pin at 3.5V and 930MHz, when tuned for a maximum output power. The FET with Z_{S2} control realizes Pout of 32.8dBm with PAE of 71% at Pin = 22dBm.

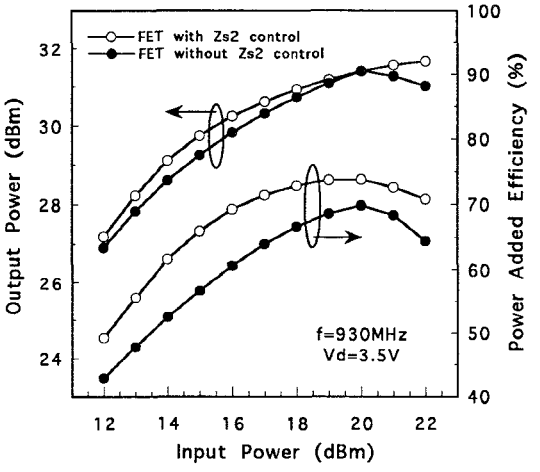


Fig. 3. Measured Pout and PAE of the FET as a function of Pin at 3.5V and 930MHz, when tuned for a maximum PAE. The FET with Z_{S2} control achieves an excellent PAE of 74% with Pout of 31.4dBm at Pin = 20dBm.

AMPLIFIER PERFORMANCE

Power performances of the FET (Wg = 12mm) were measured at a supply voltage of 3.5V and 930MHz. Figure 1 shows a circuit diagram of the newly developed power amplifier. Source and load fundamental impedances (Z_{S1}, Z_{L1}) were tuned by variable shunt capacitors connected with 50Ω microstrip line. Source and load second-harmonic impedances (Z_{S2}, Z_{L2}) were optimized with approximate short circuits. The FET was assembled in a metal-based package. The drain bias current was set to be 100mA (3% of Idss).

Measured output power (Pout) and power added efficiency (PAE) as a function of input power (Pin) are shown in Fig. 2. When the FET (with Z_{S2} control) is tuned to obtain a maximum output power, it realizes Pout of 32.8dBm with a high PAE of 71% and an associate gain of 10.8dB at Pin = 22dBm. On the other hand, the same FET without Z_{S2} control is limited to deliver a maximum output power of 32dBm with PAE of 67% at Pin = 21dBm. The FET with Z_{S2} control shows great improvement of maximum output power and PAE by 0.8dB and 4%, respectively.

The FET was then impedance-matched for a maximum PAE at Vd = 3.5V and f = 930MHz. The measured results are shown in Fig. 3. The FET with Z_{S2} control achieves an excellent PAE of 74% with Pout of 31.4dBm and an associate gain of 11.4dB at Pin = 20dBm. A high PAE over 70% is attained at a wide input power range of 17-22 dBm. The measured values of Z_{S1}, Z_{S2}, Z_{L1} and Z_{L2} for the maximum

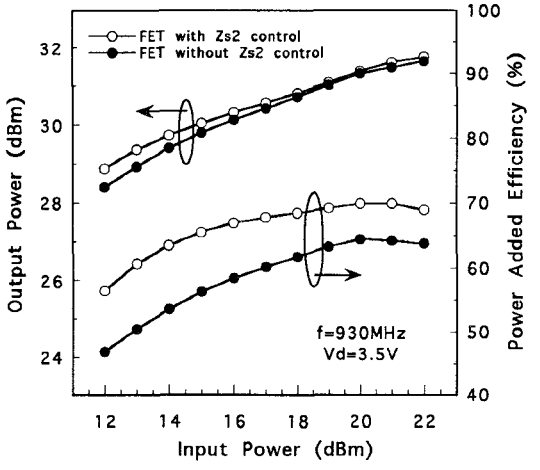
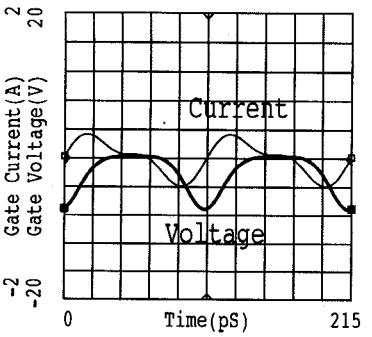


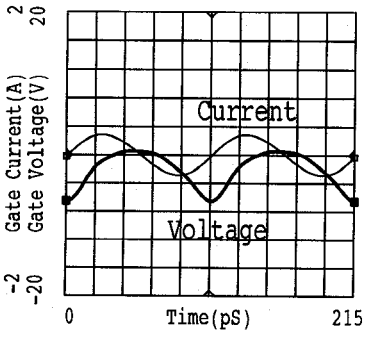
Fig. 4. Simulated Pout and PAE of the FET as a function of Pin. By optimizing Z_{S2}, PAE is improved by 5% at Pin = 20dBm. This results agree with the measured ones.

PAE were : Z_{S1} = 3.3 + j10.8 Ω, Z_{S2} = 1.2 + j11.7 Ω, Z_{L1} = 8.6 + j1.2 Ω and Z_{L2} = 1.2 + j14.5 Ω. The output power and PAE strongly depended on Z_{S2} under the same condition of Z_{S1}. When the same FET without Z_{S2} control is tuned to obtain Pout of 31.4dBm at Pin = 20dBm, a maximum PAE was limited to 70%. By optimally controlling Z_{S2}, PAE is improved by more than 4% at around the saturation output power, and by more than 8% at a lower input power range of 13-16 dBm.

Harmonic balance simulation was performed on MDS (Commercial CAD by Hewlett Packard). Simulated Pout and PAE characteristics of the FET at Vd = 3.5V and f = 930MHz



(a) with Z_{S2} control



(b) without Z_{S2} control

Fig. 5. Simulated Gate voltage/current waveforms at Pin = 20dBm under two conditions (with Z_{S2} control (a) and without Z_{S2} control (b)). The gate voltage waveform with Z_{S2} control is close to a square wave.

are shown in Fig. 4. By optimally controlling Z_{S2}, PAE of the FET is improved by 5% at an input power of 20dBm. This results which agree with the measured ones confirm the advantage of the Z_{S2} control technology for obtaining high power and high efficiency amplifiers.

Gate voltage/current waveforms were analyzed by MDS. Figure 5 shows simulated gate voltage/current waveforms at Pin = 20dBm under two conditions (with Z_{S2} control (a) and without Z_{S2} control (b)). The gate voltage waveform with Z_{S2} control (a) is close to a square wave, in comparison with that without Z_{S2} control (b). At the large-signal operation, a voltage wave inputted into the gate is well controlled from a sinusoidal wave to a quasi-square wave, by optimally terminating Z_{S2}. This quasi-square gate voltage would contribute to reduce the voltage/current switching time at the drain . This avoids the heat dissipation which occurs when the drain voltage and current exist simultaneously, and results in the significant improvement of PAE. In addition, the quasi-square gate voltage with a wide flat portion (at $Vg \approx 0V$) would provide a large current drain swing which is important to deliver an increased output power under limited voltage conditions.

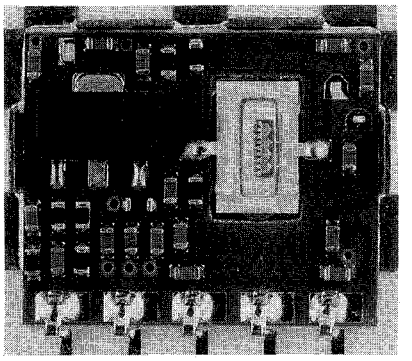


Fig. 6. A photograph of the developed two-stage GaAs power module. The volume of this module is only 0.4cc, half of that of a conventional one.

In this simulation, the drain voltage waveform with Z_{S2} control shows a peak value of 12V, while that without Z_{S2} control has a peak value of as low as 9V. This indicates the new amplifier requires higher breakdown voltage (BVgd). Under the 3.5V operating condition, BVgd of more than 14V is necessary, as considering a margin of 2V. The fabricated FET has sufficiently satisfied this requirement.

POWER MODULE

Using the new technology, a two-stage GaAs power amplifier (PA) module for cellular phones was demonstrated. Figure 6 shows a photograph of the power module. It used two kinds of GaAs MESFETs (200mW-class and 1.5W-class) with total gate width of 2mm and 12mm. A semi-flexible printed board made of PPO (Poly-Phenylene-Oxide) with high εr (10.5) and low $\tan\delta$ (0.003) is used. The volume of the power module is only 0.4cc, which is only half of that of a conventional one [5-6]. The optimum tuning of Z_{S2} is only provided with the final-stage FET, because the efficiency mainly depends on it. Second-harmonic load impedance (Z_{L2}) is also optimized in the output matching circuit in order to achieve both a high PAE and a low second-harmonic level.

Figure 7 shows measured Pout and PAE characteristics of the power module. A high PAE of 66% with Pout of 31dBm is achieved at a low supply voltage of 3.5V and Pin = 7dBm around 915-945 MHz band. By optimally controlling Z_{S2}, PAE is improved by more than 6% with the same output power of 31dBm. Supply voltage dependence of the power module is shown in Fig. 8. It maintains a high PAE of 66% at a supply voltage range of 2.8-3.5V.

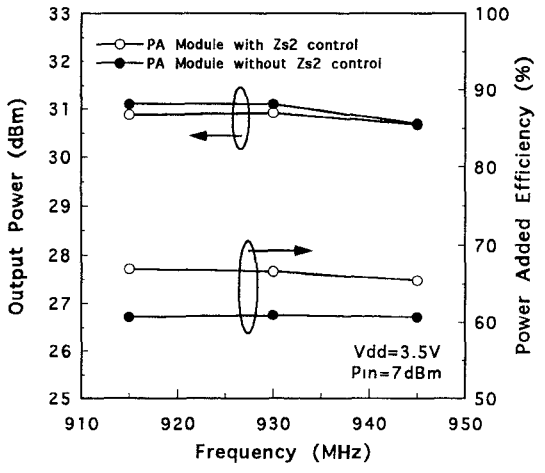


Fig. 7. Measured Pout and PAE of the power module. A high PAE of 66% with Pout of 31dBm is achieved at 3.5V and around 915-945 MHz band.

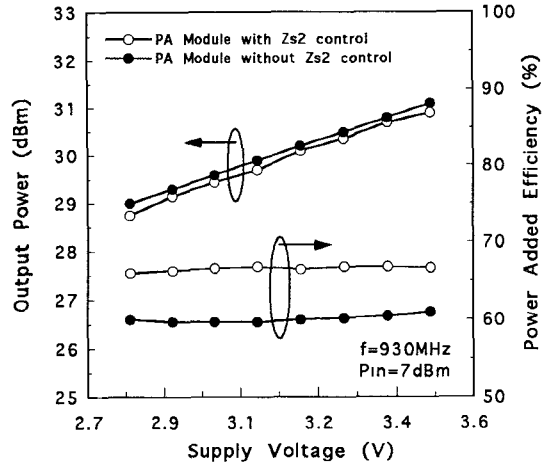


Fig. 8. Measured supply voltage dependence of the power module. It maintains a high PAE of 66% at a supply voltage range of 2.8-3.5V.

CONCLUSION

The effects of tuning second-harmonic source impedance (Z_{S2}) on Pout and PAE of the GaAs MESFET have been studied at 900MHz band. By optimally controlling Z_{S2} as well as Z_{L2}, the FET has realized Pout of 32.8dBm with PAE of 71% at Vd = 3.5V and f = 930MHz. More over, when the FET is tuned for a maximum PAE, it has achieved an excellent PAE of 74% with Pout of 31.4dBm. Using this technology, a small sized (0.4cc) two-stage power module has demonstrated. It has attained a high PAE of 66% with Pout of 31dBm at Vd = 3.5V around 915-945 MHz band. The excellent performances strongly indicate the advantage of the new technology for high power and high efficiency amplifiers.

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